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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/782,810	02/23/2004	Hiroyuki Tomimatsu	114371.01	5451
25944	7590	01/12/2006	EXAMINER	
OLIFF & BERRIDGE, PLC P.O. BOX 19928 ALEXANDRIA, VA 22320			PHAM, HOAI V	
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/782,810

Applicant(s)

TOMIMATSU, HIROYUKI

Examiner

Hoai v. Pham

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 October 2005.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11, 13-23 is/are pending in the application.
- 4a) Of the above claim(s) 14-23 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11 and 13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☐ Certified copies of the priority documents have been received.
 - 2) ☒ Certified copies of the priority documents have been received in Application No. 10/327968.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 10/26/05.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 8 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The phrase "the second wire being bonded to the other of the two second pads" is not enabled. It is not understood how the second wire being bonded to the other of the two second pads while claim 1 recited a second wire that is bonded to the lead and to one of the first pad and the second pad (the first second pad).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 10-11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Glenn et al. [U.S. Pat. 6,522,015] newly cited, in view of Chuang [U.S. Pat. 6,483,178] newly cited.

With respect to claim 1, Glenn et al. (figs. 4-5, cols. 4-5) discloses a semiconductor device, comprising:

- a die pad (470) (see col. 7, lines 25-26);
- a plurality of semiconductor chips stacked on one surface of the die pad;
- a lead (472) extending toward the die pad, the lead being a separate element from the die pad (see fig. 5 and col. 7, lines 26-27);
- a first wire (480A) that is bonded to a first pad (416A) of a first semiconductor chip (412) among the plurality of semiconductor chips and to a second pad (462A) of a second semiconductor chip (452) among the plurality of semiconductor chips;
- a second wire (474A) that is bonded to the lead and to the first pad (416A) (see fig. 5); and
- a sealing material (510) that seals the plurality of semiconductor chips (see fig. 5).

Glenn et al. fails to disclose that the sealing material (510) exposes another surface of the die pad. However, Chuang discloses the sealing material (5) exposes another surface of the die pad (1') (see fig. 2 and col. 1, lines 35-40). Therefore, it would have been obvious to one ordinary skill in the art to modify the device of Glenn et al. with exposing the bottom surface of the die pad as taught by Chuang in order to

provide the semiconductor chip with a direct heat dissipation path to the atmosphere.

With respect to claim 10, Glenn et al. discloses that the second semiconductor chip (452) being mounted on the first semiconductor chip (412), and the second wire (474A) being bonded to the lead (472A) and to the first pad (416A) (see figs. 4-5).

With respect to claim 11, Glenn et al. discloses that the first semiconductor chip (412) being a memory, and the second semiconductor chip (452) being a microprocessor (see col. 4, lines 35-44).

With respect to claim 13, Glenn et al. discloses an electronic device, comprising: the semiconductor device according to claim 1 (see figs. 4-5).

5. Claims 1-7, 9 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mess et al. [U.S. Pat. 6,900,528] previously applied.

With respect to claim 1, Mess et al. (fig. 13, cols. 6-9) discloses a semiconductor device, comprising:

- a plurality of semiconductor chips stacked on one surface of a substrate (70);
- a first wire (62) that is bonded to a first pad (54A) of a first semiconductor chip (60A) among the plurality of semiconductor chips and to a second pad (54B) of a second semiconductor chip (60B) among the plurality of semiconductor chips;

a second wire (62) that is bonded to the substrate (70) and to the second pad (54B); and

a sealing material (84) that seals the plurality of semiconductor chips and exposes another surface of the substrate.

Mess et al. (fig. 13) does not disclose that the substrate (70) is a lead extending toward a die pad, the lead being a separate element from the die pad. However, Mess et al. (fig. 12A and col. 7, lines 20-23) disclose that the substrate (70) can be a lead (102A, 102B) extending toward a die pad (98), the lead being a separate element from the die pad. Therefore, it would have been obvious to one ordinary skill in the art to modify the substrate (70) of Mess et al. in fig. 13 with the lead being a separate element from the die pad as being claimed above because as taught by Mess et al. the invention can be applied to the multi-chip package types semiconductor devices formed on the lead frame (see fig. 12A, col. 5, lines 60-65 and col. 7, lines 20-23).

With respect to claim 2, Mess et al. discloses that the second semiconductor chip (60B) being mounted on the first semiconductor chip (60A), and the second wire (62) being bonded to the lead and to the second pad (see fig. 13).

With respect to claim 3, Mess et al. discloses that the second wire (62) being lead out to pass above the first wire (see fig. 13).

With respect to claim 4, Mess et al. discloses that the second wire (62) being lead out to traverse the first wire (see fig. 13).

With respect to claim 5, Mess et al. discloses that the second wire (62) being overlapped with and bond to the first wire on the second pad (54B) (see fig. 13).

With respect to claim 6, Mess et al. discloses that the second wire (62) including a ball formed on a tip thereof, and the ball being press-bonded to the first wire (see fig. 13 and col. 6, lines 65-67).

With respect to claim 7, Mess et al. discloses that the second wire (62) being bonded to the second pad (54B) that is bonded to the first wire, while avoiding a bonded section of the first wire (see fig. 13).

With respect to claim 9, Mess et al. discloses that the second pad (54B) being provided with a bump, and the first wire and the second wire being bonded to the second pad through the bump (see fig. 13).

With respect to claim 13, Mess et al. discloses an electronic device, comprising: the semiconductor device according to claim 1 (see fig. 12A).

Response to Arguments

6. Applicant's arguments with respect to claims 1-11 and 13 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

8. A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai v. Pham whose telephone number is 571-272-1715. The examiner can normally be reached on M-F.

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10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



HOAI PHAM
PRIMARY EXAMINER